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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASINGTON, DC 20004-2128

EXAMINER	
SHAPIRO, LEONID	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/777,693	KOYAMA ET AL.
	Examiner	Art Unit
	Leonid Shapiro	2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-104* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of claims 1, 19, 36, 54, 71, 80, 88, 97: "a multiple of m shift registers" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 19-25, 71-79, 80-87 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima (US Patent No. 6,256,079 B1) in view of Lewis (US Patent No. 5,589,847) and Luder et al. (US Patent No. 5,642,117).

As to claim 1, Matsushima teaches an image display device (See Fig. 6, Col, 1, Lines 17-31), comprising: a pixel array portion including k (k is an integer not less than 2) signal lines (See Fig..6, item 120, Col. 10, Lines 17-31), a plurality of scan lines (See Fig. 6, item 116, Col. 10, Lines 17-31), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines

intersect with each other (See Fig. 6, item 36, Col. 10, Lines 31-36), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 6, item 35, Col. 10, Lines 31-36); a signal line driver circuit for driving the k signal lines (See Fig. 6, item 33, Col. 10, Lines 17-31) and a scan line driver circuit for driving the plurality of scan lines (See Fig. 6, item 32, Col. 10, Lines 17-31), wherein signal line driver includes shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) which is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter

circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima and Lewis apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 2, Lewis teaches the number of the D/A converter circuit k/n, if the k-number of signal lines and n-number of signal lines driven by the particular D/A (See Fig. 15A, item 550).

As to claim 3, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 4-7, Lewis teaches the storage circuit is a latch circuit with analog switch (See Fig. 15, item 515), holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 8, Lewis teaches liquid crystal display (See Col. 1, Line 15).

As to claim 19, Matsushima teaches an image display device (See Fig. 6, Col. 1, Lines 17-31) comprising: a pixel array portion including plurality signal lines (See Fig. 6, item 120, Col. 10, Lines 17-31), a plurality of scan lines (See Fig. 6, item 116, Col. 10, Lines 17-31), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other (See Fig. 6, item 36, Col. 10, Lines 31-36), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 6, item 35, Col. 10, Lines 31-36); a signal line driver circuit for driving the k signal lines (See Fig. 6, item 33, Col. 10, Lines 17-31) and a scan line driver circuit for driving the plurality of scan lines (See Fig. 6, item 32, Col. 10, Lines 17-31), wherein signal line driver includes a multiple of m (m is a natural number) shift registers, (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) which is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines, wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted, the inputted digital picture signals are shifted in the shift register until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into storage circuits by a latch signal, is repeated n times in a time corresponding to one horizontal scan period.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), plurality of storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48), wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted, the inputted digital picture signals are shifted in the shift register until they are outputted to the corresponding storage circuit by a latch signal, is repeated n times in a

time corresponding to one horizontal scan period (See Fig. 15A, items 505, 515, 255, 520, 550, in description See Col. 5, Lines 60-67 and Col. 6, Lines 8-26).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver in operation as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima and Lewis apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 20, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 21-24, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig.

14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 25, Lewis teaches a liquid crystal display (See Col.1, Line 15).

As to claim 71, Matsushima teaches a signal line driver circuit (See Fig. 6, item 33, Col. 1, Lines 17-30) of an image display device (See Fig. 6, Col, 1, Lines 17-31) for driving k (k is an integer not less than 2) signal lines (See Fig. 6, item 120, Col. 1, Lines 17-30) comprising: shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less

than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima and Lewis apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 72, Lewis teaches the number of the D/A converter circuit k/n, if the k-number of signal lines and n-number of signal lines driven by the particular D/A (See Fig. 15A, item 550).

As to claim 73, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 74-77, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 78, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a polysilicon thin transistor (See Abstract).

As to claim 79, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a single crystal transistor (See Abstract).

As to claim 80, Matsushima teaches a signal driver circuit (See Fig. 6, item 33, Col. 1, Lines 17-31) of an image display device (See Fig. 6, Col. 1, Lines 17-31) for driving a plurality of signal lines (See Fig. 6, item 120, Col. 1, Lines 17-31), the signal line driver circuit comprising: a multiple of m (m is a natural number) shift registers, (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, a plurality of storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal

lines, wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted, the inputted digital picture signals are shifted in the shift register until they are outputted to the corresponding storage circuits, and the shifted digital picture signals are taken into storage circuits by a latch signal, is repeated n times in a time corresponding to one horizontal scan period.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), plurality of storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48), wherein an operation in which the digital picture signals are inputted to the respective shift registers, the inputted, the inputted digital picture signals are shifted in the shift register until they are outputted to the corresponding storage circuit by a latch signal, is repeated n times in a time corresponding to one horizontal scan period (See Fig. 15A, items 505, 515, 255, 520, 550, in description See Col. 5, Lines 60-67 and Col. 6, Lines 8-26).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver in operation as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for

integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima and Lewis apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 81, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 82-85, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 86, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a polysilicon thin transistor (See Abstract).

As to claim 87, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a single crystal transistor (See Abstract).

3. Claims 36-43, 54,-60, 88-96, 97-104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima in view of Lewis, Luder et al. and Kinoshita et al. (US Patent No. 5,771,031).

As to claim 36, Matsushima teaches an image display device (See Fig. 6, Col, 1, Lines 17-31), comprising: a pixel array portion including k signal lines (See Fig. 6, item 120, Col. 10, Lines 17-31), a plurality of scan lines (See Fig. 6, item 116, Col. 10, Lines 17-31), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other (See Fig. 6, item 36, Col. 10, Lines 31-36), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 6, item 35, Col. 10, Lines 31-36); a signal line driver circuit for driving the k signal lines (See Fig. 6, item 33, Col. 10, Lines 17-31) and a scan line driver circuit for driving the plurality of scan lines (See Fig. 6, item 32, Col. 10, Lines 17-31), wherein signal line driver includes shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) which is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter

circuits for converting output signals of the storage circuits into analog signals, and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show a pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3).

Kinoshita et al. teaches pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3) (See Fig. 1, items 2, 151, 103, 113, from Col. 4, Lines 66 to Col. 5, Line 6).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement RGB pixels and signals lines as shown by Kinoshita et al. in the Matsushima and Lewis apparatus in order to maintain the memory capacity required for block-driving of each pixel to be small (See Col. 4, Lines 46-49 in the Kinoshita et al. reference).

Lewis, Matsushima and Kinoshita et al. do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima, Lewis and Kinoshita et al. apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 37, Lewis teaches the number of the D/A converter circuit k/n, if the k-number of signal lines and n-number of signal lines driven by the particular D/A (See Fig. 15A, item 550).

As to claim 38, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 39-42, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claims 43 Lewis teaches liquid crystal display (See Col. 1Line 15).

As to claim 54, Matsushima teaches an image display device (See Fig. 6, Col, 1, Lines 17-31), comprising: a pixel array portion including k signal lines (See Fig. 6, item 120, Col. 10, Lines 17-31), a plurality of scan lines (See Fig. 6, item 116, Col. 10, Lines 17-31), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other (See Fig. 6, item 36, Col. 10, Lines 31-36), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 6, item 35, Col. 10, Lines 31-36); a signal line driver circuit for driving the k signal lines (See Fig. 6, item 33, Col. 10, Lines 17-31) and a scan line driver circuit for driving the plurality of scan lines (See Fig. 6, item 32, Col. 10, Lines 17-31), wherein signal line driver includes shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) which is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n

(n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show a pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3), one horizontal scan period including R, G, B periods with R,G and B shift registers an outputs to the latch.

Kinoshita et al. teaches pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3) (See Fig. 1, items 2, 151, 103, 113, from Col. 4, Lines 66 to Col. 5, Line 6).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement RGB pixels and signals lines as shown by Kinoshita et al. and divide one horizontal scan period including R, G, B periods with R,G and B shift registers an outputs to the latch in the Matsushima and Lewis apparatus in order to maintain the memory capacity required for block-driving of each pixel to be small (See Col. 4, Lines 46-49 in the Kinoshita et al. reference).

Lewis, Matsushima and Kinoshita et al. do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima, Lewis and Kinoshita et al. apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 55, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 56-59, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 60 Lewis teaches liquid crystal display (See Col. 1Line 15).

As to claim 88, Matsushima teaches a signal line driver circuit (See Fig. 6, item 33, Col. 1, Lines 17-31) of an image display device (See Fig. 6, Col, 1, Lines 17-31), the signal line driver circuit comprising shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) which is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less

than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show a pixel array portion including k (k is a multiple of 3), signal lines corresponding to R,G, and B colors and (n is a multiple of 3).

Kinoshita et al. teaches pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3) (See Fig. 1, items 2, 151, 103, 113, from Col. 4, Lines 66 to Col. 5, Line 6).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement RGB pixels and signals lines as shown by Kinoshita et al. in the Matsushima and Lewis apparatus in order to maintain the memory capacity required for block-driving of each pixel to be small (See Col. 4, Lines 46-49 in the Kinoshita et al. reference).

Lewis, Matsushima and Kinoshita et al. do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima, Lewis and Kinoshita et al. apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 89, Lewis teaches the number of the D/A converter circuit k/n, if the k-number of signal lines and n-number of signal lines driven by the particular D/A (See Fig. 15A, item 550).

As to claim 90, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 91-94, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 95, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a polysilicon thin transistor (See Abstract).

As to claim 96, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a single crystal transistor (See Abstract).

As to claim 97, Matsushima teaches a signal driver circuit (See Fig. 6, item 33, Col. 1, Lines 17-31) of an image display device (See Fig. 6, Col, 1, Lines 17-31) for driving signal lines, the signal line driver circuit comprising shift registers, the number of shift registers being a multiple of m (m is natural number) (See Fig. 7, items 331-334, Col.2, Lines 20-36). Notice, that number of shift registers is 4 or 8 (See Col. 2, Lines 29-35) is multiple of natural number 2 or 4.

Matsushima does not show shift registers to which m-bit (m is a natural number) digital picture signals are inputted, m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers, a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals, and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines.

Lewis teaches shift registers to which m-bit (m is a natural number) digital picture signals are inputted (See Fig. 15A item 505, Col. 10, Lines 22-35), m x k/n (n is an integer of not less than 2) storage circuits for storing output signals of the shift registers (See Fig. 15A, items 515a, 515b, 515c, Col. 10, Lines 22-35) a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (See Fig. 15A items 255a, 255b, 255c, Col. 22-35), and k/n (n is an integer of not less than 2) signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 15A, items 520a, 520b, 520c, Col. 10, Lines 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by Lewis in the Matsushima apparatus in order to fabricate interface circuit suitable for integration with other circuit elements in large area electronic device (See Col. 4, Lines 46-49 in the Lewis reference).

Lewis and Matsushima do not show a pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3), one horizontal scan period including R, G, B periods with R,G and B shift registers outputs to the latch.

Kinoshita et al. teaches pixel array portion including k (k is a multiple of 3) signal lines corresponding to R,G, and B colors and (n is a multiple of 3) (See Fig. 1, items 2, 151, 103, 113, from Col. 4, Lines 66 to Col. 5, Line 6).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement RGB pixels and signals lines as shown by Kinoshita et al. and divide one horizontal scan period including R, G, B periods with R,G and B shift registers outputs to the latch in the Matsushima and Lewis apparatus in order to maintain the memory capacity required for block-driving of each pixel to be small (See Col. 4, Lines 46-49 in the Kinoshita et al. reference).

Lewis, Matsushima and Kinoshita et al. do not show ramp type D/A converter circuit comprises a bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Matsushima, Lewis and Kinoshita et al. apparatus in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 98, Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

As to claims 99-102, Lewis teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Fig. 14A, 14B, items Q1, Q2, nQ1, nQ2, 400, 420, 430, in description See Col. 9, 51-67 and Col.10, Lines 1-21).

As to claim 103, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a polysilicon thin transistor (See Abstract).

As to claim 104, Lewis teaches a circuit, wherein the driver circuit of the image display device is formed of a single crystal transistor (See Abstract).

4. Claims 9, 26, 44, 61 rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis, Matsushima and Kinoshita et al. and Luder et al. as aforementioned in

claims 1, 19, 36, 54 in view of Friend et al (US Patent No. 5,247,190), sited by the applicant.

Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a display using electroluminescence (EL) material.

Friend et al. shows a display using electroluminescence (EL) material n (See Fig. 3, items 3-5, in description See Col.8, Lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to use materials as shown by Friend et al in the Lewis, Matsushima, Kinoshita et al. and Luder et al. apparatus in order to increase the range of applications.

5. Claims 10-18, 27-35, 45-53, 62-70 rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis, Matsushima and Kinoshita et al. and Luder et al. as aforementioned in claims 1,19, 36, 54 in view of Matsueda et al (US Patent No. 6,384,806 B1).

As to claims 10, 27, 45, 62, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a portable telephone, which uses the image display device.

Matsueda et al. shows a portable telephone, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the portable telephone as shown by Matsueda et al. in order to increase the range of applications.

As to claims 11, 28, 46, 63, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a video camera, which uses the image display device.

Matsueda et al. shows a video camera, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 8-15).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the video camera as shown by Matsueda et al. in order to increase the range of applications.

As to claims 12, 29, 47, 64, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a personal computer, which uses the image display device.

Matsueda et al. shows a personal computer, which uses the image display device (See Fig. 20, in description See Col. 22, Lines 38-43). It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Suzuki, Akiyama et al. and Luder et al. apparatus in the personal computer as shown by Matsueda et al. in order to increase the range of applications.

As to claims 13, 30, 48, 65, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a head mounted display, which uses the image display device.

Matsueda et al. shows a head mounted display, which uses the image display device (See Fig. 21, in description See Col. 22, Lines 57-65).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus

in the head mounted display as shown by Matsueda et al. in order to increase the range of applications.

As to claims 14, 31, 49, 66, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a television, which uses the image display device.

Matsueda et al. shows a television, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 8-17).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the television as shown by Matsueda et al. in order to increase the range of applications.

As to claims 15, 32, 50, 67, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a portable book, which uses the image display device.

Matsueda et al. shows a portable book, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 8-17).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the portable book as shown by Matsueda et al. in order to increase the range of applications.

As to claims 16, 33, 51, 68, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a CVD player, which uses the image display device.

Matsueda et al. shows a CVD player, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 8-17).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the CVD player as shown by Matsueda et al. in order to increase the range of applications.

As to claims 17, 34, 52, 69, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a digital camera, which uses the image display device.

Matsueda et al. shows a CVD player, which uses the digital camera device (See Fig. 19-22, in description See Col. 23, Lines 8-17).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the digital camera as shown by Matsueda et al. in order to increase the range of applications.

As to claims 18, 35, 53, 70, Lewis, Matsushima and Kinoshita et al. and Luder et al. do not teach a projector, which uses the image display device.

Matsueda et al. shows a CVD player, which uses the projector device (See Fig. 19, in description See Col. 22, Lines 3-35).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Lewis, Matsushima and Kinoshita et al. and Luder et al. apparatus in the projector as shown by Matsueda et al. in order to increase the range of applications.

Response to Amendment

6. Applicant's arguments filed on 03-18-04 with respect to claims 1-104 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 05-27-04

VIJAY SHANKAR
PRIMARY EXAMINER